CLAIMS

What is claimed is:

1. An apparatus comprising:

a plurality of processors coupled to a controller and a memory;

the controller to execute a debug process, said debug process attaches at least one breakpoint bit field to each of a plurality of instructions.

2. The apparatus of claim 1, wherein said breakpoint bit allows a breakpoint to be one of set and not set for each of said plurality of instructions.

3. The apparatus of claim 2, wherein a breakpoint bit set for an instruction is associated with the address of the instruction.

4. The apparatus of claim 1, and said controller attaches at least three debug register bit fields to at least one control status register, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

5. The apparatus of claim 4, said single step field allows a set of instructions to each be single-stepped through one cycle at a time.

6. The apparatus of claim 4, said debug enable field one of enables and disables a debug mode.

7. The apparatus of claim 1, wherein at least one instruction loads content of at least one register into an instruction memory coupled to said at least one processor via a bus.

8. The apparatus of claim 7, wherein content of said instruction memory is loaded into a register coupled to said at least one processor.

9. The apparatus of claim 1, wherein internal states of each of said plurality of processors are accessible through said debug process.

10. A system comprising:

a plurality of image signal processors (ISPs), each ISP including a plurality of processor elements (PEs), the plurality of ISPs including:

a debug instruction register coupled to a first mux element,

an instruction memory coupled to an instruction register,

a decoder coupled to said instruction register,

an execution unit coupled to said decoder,

a debug executive unit coupled to said instruction memory, and

a second mux element coupled to said execution unit and a plurality of local registers,

wherein the decoder to decode at least one breakpoint bit field of each of a plurality of instructions.

11. The system of claim 10, wherein said plurality of ISPs arranged in a matrix pattern and each having quad-ports.

12. The system of claim 11, said plurality of PEs each coupled to a register file switch.

13. The system of claim 10, the decoder to decode at least three debug register bit fields of a control status register, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

14. The system of claim 13, said single step field allows a set of instructions to each be single stepped through one instruction at a time.

15. The system of claim 10, wherein at least one instruction loads content of said debug instruction register into said instruction memory.

16. The system of claim 15, wherein content of said instruction memory is loaded into said debug instruction register.

17. The system of claim 16, wherein internal states of said plurality of PEs are accessible through said debug instruction register.

18. An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

attaching at least one breakpoint bit field to each of a plurality of instructions,

attaching at least three debug register bit fields to at least one control status register.

19. The apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of said breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set.

20. The apparatus of claim 18, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

21. The apparatus of claim 20, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a run field bit, and

running a set of instructions if said state of said run field bit is set, and

stopping a set of instructions if said state of said run field bit is not set.

22. The apparatus of claim 21, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a single step bit,

single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

23. The apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

loading content of at least one register into an instruction memory,

loading content of said instruction memory into the at least one register, and

accessing internal states of each of a plurality of processors through said debug process.

24. A method comprising:

attaching at least one breakpoint bit field to each of a plurality of instructions,

attaching at least three breakpoint register bit fields to at least one control status register,

wherein the attached breakpoint bit field is an additional field added to each instruction.

25. The method of claim 24, further comprising determining a state of said breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set.

26. The method of claim 24, further comprising:

running a debug process on a host device, and

entering debug commands through a graphical user interface.

27. The method of claim 24, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

28. The method of claim 24, further comprising:

determining a state of a single-step bit,

entering commands for single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

29. The method of claim 24, further comprising:

loading content of at least one register into an instruction memory,

loading content of said instruction memory into the at least one register, and

accessing internal states of each of a plurality of processors through said debug process, wherein accessing includes reading state values and overwriting state values.